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EXAMINER	
YUSHINA, GALINA G	
ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/583,501	FUJIKAWA ET AL.	
	Examiner	Art Unit	
	GALINA YUSHINA	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *10-17 and 19* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *10-17 and 19* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's response to the Advisory Action filed on 10/19/11 is acknowledged. In the response to the Examiner' indicated allowable subject matter of Claim 10 (in the Office Action mailed 10/04/2011), the Applicant cancelled Claims 1-9.

However, the indicated allowability of Claim 10 is withdrawn in view of the newly discovered reference(s) for Claim 10, Beasom (US 4,873,564). Rejections based on this reference follow.

2. Claim 18 was cancelled earlier. Claims 10-17 and 19 are examined on merits herein.

Claim Rejections - 35 USC § 102

3. **The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102** that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 10 and 19 are rejected under 35 U.S.C. 102(b)** as being anticipated by Beasom (US 4,873,564).

5. **In re Claim 10,** Beasom teaches a junction field-effect transistor comprising (Fig. 3 and Fig. 4):

- a first conductivity type (n-type, column 5, lines 16-17) first semiconductor layer (15) having a substantially flat cross- sectional shape (as is shown in Fig. 4) and having a channel region (26, column 5, line 27),

- a buffer layer (24, column 5, line 14) of a second conductivity type (p-type) formed on the channel region (26) in the first conductivity type first semiconductor layer (15), the buffer layer (26) having a substantially flat cross-sectional shape (as shown in Fig. 4), and
- a second conductivity type doped region (25, column 5, lines 18-19) extending into the first conductivity type first semiconductor layer (15) to a top surface of the buffer layer (24), but not extending through the buffer layer (24), wherein
- a second conductivity carrier concentration (10^{14} cm^{-3}, column 6, line 15) in the buffer layer (24) is lower than a first conductivity carrier concentration ($2x10^{14}$ cm^{-3}, column 6, line 19) in the first conductivity type first semiconductor layer.

6. **In re Claim 19**, Beasom teaches the junction field-effect transistor according to Claim 10 as cited above.

Beasom further teaches (Fig. 3) that wherein the second conductivity type doped region (25, column 5, lines 18-19) does not extend into the buffer layer (24, column 5, line 14).

Claim Rejections - 35 USC § 103

7. **The following is a quotation of 35 U.S.C. 103(a)** which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 11 and 15 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Beasom in view of Sriram (US 2003/0075719).

9. **In re Claim 11**, Beasom teaches the junction field-effect transistor of Claim 10 as cited above.

Beasom does not teach that the first conductivity type first semiconductor layer is composed of silicon carbide.

Sriram teaches (Fig. 1) that the first conductivity type first semiconductor layer (14, 16, paragraphs 0030-0031) is composed of silicon carbide.

Beasom and Sriram teach analogous arts directed towards field effect transistors, and one of ordinary skill in the art would have had a reasonable expectation of success to modify the Beasom transistor in view of the Sriram transistor because they are from the same field of endeavor.

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify the Beasom device by creating its semiconductor layers of silicon carbide (per Sriram) in order to create a device capable of operation at higher temperature and a higher power (Sriram, paragraph 0009).

10. **In re Claim 15**, Beasom teaches the junction field-effect transistor of Claim 10 as cited above, including the first conductivity type first semiconductor layer.

Beasom further teaches (Fig. 3) that the first conductivity type first semiconductor layer (15, column 5, lines 16-17) is formed on one main surface (a top surface) of a semiconductor substrate (10).

Beasom does not teach a semiconductor substrate that composed of a silicon carbide.

Sriram teaches (Fig. 1) that a semiconductor substrate (10) is composed of silicon carbide (paragraph 0028).

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify the Beasom device by creating its semiconductor layers of silicon carbide (per Sriram) in order to create a device capable of operation at higher temperature and a higher power (Sriram, paragraph 0009).

11. **Claim 12 is rejected under 35 U.S.C. 103(a)** as being unpatentable over *Beasom (US 4,873,564)* in view of Nonaka et al. (US 4,807,011).

12. **In re Claim 12,** Beasom teaches a junction field-effect transistor of Claim 10 as cited above.

Beasom does not teach the transistor further comprising another second conductivity type doped region under the channel region.

Nonaka teaches the junction field-effect transistor further comprising (Fig. 3) another second conductivity type (p-type) doped region (10, column 4, lines 65-66) under the channel region (18a, column 5, line 39.

Beasom and Nonaka teach analogous arts directed towards junction field effect transistors, and one of ordinary skill in the art would have had a reasonable expectation of success to modify the Beasom transistor in view of the Nonaka transistor because they are from the same field of endeavor.

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify the Beasom/Nonaka device of Claim 10 by including another second conductivity type doped region in order to increase a speed of the device operation (Nonaka, column 2, lines 62-64).

13. **Claims 13 and 14 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Beasom in view of Nonaka and Kumar et al. (US 2002/0139992).

14. **In re Claim 13**, Beasom teaches the junction field-effect transistor according to Claim 10 as cited above, including the first conductivity type semiconductor layer.

Beasom does not teach the transistor comprising of:

- another buffer layer of the first conductivity type under the channel region, and
- another second conductivity type doped region that reaches the other buffer layer and is in a first conductivity type second semiconductor layer under the other buffer layer, wherein

- a first conductivity type carrier concentration in the other buffer layer is lower than a first conductivity type carrier concentration in the first conductivity type first semiconductor layer.

Nonaka teaches the device further comprising (Fig. 3):

- another buffer layer (12, column 4, line 68) of the first conductivity type (n-type) under the channel region (18a, column 5, line 39),
- another second conductivity type doped region (10, column 5, line 6) that reaches the other buffer layer (12) and is under the other buffer layer (12), wherein
- a first conductivity type (n-type) carrier concentration in the other buffer layer (12, having a carrier concentration up to $1x10^{20}/cm^3$, column 4, line 68 and column 5, line 1) is lower than a first conductivity type carrier concentration in the first conductivity type semiconductor layer (18, since layer 18 includes region 30, having a carrier concentration up to $1x10^{21}/cm^3$, column 6, line 6).

Nonaka does not teach in the embodiment of Fig. 3 that the other buffer layer is in a first conductivity type (n-type) second semiconductor layer; he teaches another second conductivity (p-type) semiconductor layer (10, as the substrate). However, Nonaka states that a substrate is made of, "for example", a p-type silicon (column 4, lines 65-66). Nonaka further teaches (Fig. 1) that a substrate (2, column 3, line 31) has a first conductivity type.

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify the Beasom device by adding another buffer layer of the first

conductivity type under the channel region and another second conductivity type doped region that reaches the other buffer layer in order to increase a speed of the device operation (Nonaka, column 2, lines 62-64).

Beasom, as modified per Nonaka, does not teach that another second conductivity type doped region is in a first conductivity type second semiconductor layer.

Kumar teaches (Fig. 2) the other buffer layer (4, paragraph 0039) is in a first conductivity type (n-type) second semiconductor layer (1 and 2, paragraph 0038, wherein 1 is a substrate).

Beasom and Kumar teach analogous arts directed towards junction field effect transistors, and one of ordinary skill in the art would have had a reasonable expectation of success to modify the Beasom/Nonaka transistor in view of Kumar because they are from the same field of endeavor.

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify the Beasom/Nonaka' device by creating another first conductivity type semiconductor body (per Kumar and per Nonaka' device of Fig. 1) in order to create a high-power and high-frequency device (Nonaka, column 4, lines 14-18) comprising a first type conductivity substrate device wherein this type of substrate conductivity is required for other devices built on the same substrate.

15. **In re Claim 14**, Beasom, as modified per Nonaka and Kumar, teaches the junction field-effect transistor of Claim 13 as cited above.

Beasom does not teach that the first conductivity type carrier concentration in the other buffer layer is not more than one tenth of the first conductivity type carrier concentration in the first conductivity type first semiconductor layer.

Nonaka further teaches (Fig. 3) that where the first conductivity type (n-type) carrier concentration in the other buffer layer (12, which has a carrier concentration in the range of $1x10^{18}/cm^3$ to $1x10^{20}/cm^3$, column 4, line 68 and column 5, line 1) is not more than one tenth of the first conductivity type carrier concentration in the first conductivity semiconductor layer (18, since layer 18 includes region 30, having a carrier concentration in the range of $1x10^{18}/cm^3$ to $1x10^{21}/cm^3$, column 6, line 6).

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify the Beasom/Nonaka/Kumar device of Claim 13 per Nonaka (as shown for Claim 14) in order to increase a speed of the device operation (Nonaka, column 2, lines 62-64).

16. **Claim 16 is rejected under 35 U.S.C. 103(a)** as being unpatentable over Beasom/Sriram in view of Zhao (US 6,841,812).

17. **In re Claim 16**, Beasom, as modified per Sriram, teaches the junction field-effect transistor of Claim 15 as cited above.

Beasom/Sriram does not explicitly teach the transistor further comprising: a gate electrode on the surface of the second conductivity type doped region, an electrode, either a source electrode or a drain electrode, on the surface of the first conductivity

type first semiconductor layer, and another electrode, either a drain electrode or a source electrode, on another main surface of the semiconductor substrate.

Zhao teaches a junction field effect transistor comprising (Fig. 1A):

- a gate electrode (61, column 7, lines 51-52) on the surface of the second conductivity type (p-type) doped region (60, column 5, lines 20-21),
- an electrode, either a source electrode or a drain electrode (71, a source electrode, column 5, line 25), on the surface of the first conductivity type (n-type) first semiconductor layer (40, column 5, line 7), and
- another electrode, either a drain electrode or a source electrode (11, a drain electrode, column 5, lines 9-11), on another main surface of a semiconductor substrate (20).

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify the Beasom/Sriram device by providing it with a gate electrode on the surface of the second conductivity type doped region, with a source electrode on one surface of the semiconductor substrate, and with a drain electrode on another main surface of the semiconductor substrate (that has an N^+ region 12) (per Fig. 1 of Nonaka and per Zhao) in order to enable (or to make easier) an access to the drain electrode of the device and to provide its operability.

18. **Claim 17 is rejected under 35 U.S.C. 103(a)** as being unpatentable over Beasom/Sriram in view of Nonaka.

19. **In re Claim 17**, Beasom/Sriram teaches the junction field-effect transistor according to Claim 15 as cited above.

Beasom does not explicitly teach a transistor further comprising:

- a gate electrode on the surface of the second conductivity type doped region, and
- a source electrode and a drain electrode on the surface of the first conductivity type first semiconductor layer.

Sriram teaches (Fig. 1):

- a source electrode (28, paragraph 0038) and a drain electrode (30, paragraph 0038) on the surface of the first conductivity type first semiconductor layer (14, 16, paragraph 0032).

It would have been obvious for one of ordinary skill in the art at the time of the invention to provide for the Beasom/Sriram device a source electrode and a drain electrode allowing a good ohmic contact for contact with other devices and circuits.

Beasom, as modified per Sriram, does not teach that a gate electrode is on the surface of the second conductivity type doped region.

Nonaka teaches the transistor comprising:

- a gate electrode (40, column 6, lines 18-20) on the surface of the second conductivity type (p-type) doped region (26, column 5, lines 44-45),

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify the Beasom/Sriram device by providing a gate electrode on the surface of the second conductivity type doped region enabling a good ohmic contact with external circuits.

Response to Arguments

The Applicant did not present any arguments due to suggested allowance of Claims 10-17 and 19.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GALINA YUSHINA whose telephone number is (571)-270-7440. The examiner can normally be reached on Monday through Friday, 7:30 to 5, 5/4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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